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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,332	11/08/2001	Andrew Marshall	TI-31484	3238

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,332	MARSHALL, ANDREW	
	Examiner	Art Unit	
	Matthew E Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on May 17, 2004.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 10 has been amended and states that bodies of matched transistors "are not tied to any fixed potential through a low impedance path." The specification is not enabling for the limitation because it does not mention that the bodies are not tied to any fixed potential. Furthermore, the specification does not mention a low impedance path and thus does not support the added limitation. It is shown in the specification that the bodies are totally isolated from other components or devices however it still does not mean that there can't be a potential tied to the body. It seems that if a source or drain is tied to a fixed potential, then the body of the transistor is also tied to a fixed potential. It is unclear how this is possible since there is no mention of such a limitation. For purpose of a prior art rejection, the examiner will interpret the limitation to mean that

the body is isolated from other components. This interpretation will remain until evidence is shown in the specification that such a configuration is possible.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 6, 9, and 16-19 are rejected under 35 U.S.C. 102(a) as being anticipated by Flaker et al. (US 6,133,608).

In re claim 6, Flaker et al. shows (fig. 10B or 20) an integrated semiconductor-on-insulator circuit structure comprising a pair of transistors in a circuit stage which requires matched behavior of said pair (col. 7, lines 15-24). and a physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors (col. 4, lines 60-67). Flaker et al. does not specifically disclose that the circuit stage is an analog circuit stage. However, Flaker discloses that the invention is desirable in certain circuits such as a differential amplifier which is a type of analog circuit. A physical connection of metallic material which provides thermal conduction between respective bodies of said pair of transistors is disclosed in an alternative embodiment in which metal may be used instead of the silicon body link to provide connection between the two transistor bodies (col. 6, line 53 – col. 7, line 4). An

insulating layer (48) is beneath said pair and an insulating barrier (69) substantially surrounding said pair extends to said insulating layer.

In re claim 9, Flaker discloses (col. 7, lines 1-4) that said physical connection comprises metal interconnects between said transistors of said pair.

In re claim 16, Flaker et al. discloses a method of circuit operation, comprising the steps of providing a pair of matched transistors, in a circuit stage which requires matched behavior of said pair (col. 7, lines 15-24) and providing a physical connection of material which provides thermal conduction between respective bodies of said pair of transistors (col. 7, lines 5-14) and surrounding said circuit stage with an insulating material (col. 6, lines 35-53).

In re claim 17, Flaker et al. discloses (col. 7, lines 5-14) that said physical connection is of a semiconductor material.

In re claim 18, Flaker et al. does not specifically disclose that the circuit stage is an analog circuit stage. However, Flaker discloses that the invention is desirable in certain circuits such as a differential amplifier which is a type of analog circuit.

In re claim 19, Flaker does not specifically state that said physical connection does not carry current during normal operation of said circuit stage. Flaker implies that the body link does not carry current because it is an undoped region of silicon material (col. 5, lines 1-10). Intrinsic silicon is a poor conductor of electricity. In order for it to conduct, an extremely high voltage would have to be applied to the silicon. Such a voltage is too high for typical FETs and would thus destroy them. Therefore, during normal operation, the body link (32) does not carry current. Furthermore, the

combination of the isolation oxide (40 in fig. 10B) and the body link (32) resist punch through between adjacent diffusions (col. 5, lines 53-65) and therefore act as a barrier or blocking region.

Claims 10-13, and 15, as far as understood, are rejected under 35 U.S.C. 102(a) as being anticipated by Houston et al. (US 6,037,808).

In re claim 10 (as far as understood), Houston et al. shows (figs. 5a – 5d) an integrated semiconductor-on-insulator circuit structure, comprising a plurality of matched transistors in an analog circuit stage which requires matched behavior of said transistors (col. 9, lines 1-18) wherein respective bodies of said transistors are formed from different semiconductor sections (sections of transistors T4 and T5 in figs. 5a), said sections being formed on an insulating layer (Ox) and at least partially separated by insulating material (see hash marks between sections of T4 and T5 in fig. 5a). The bodies are thermally coupled by a connection of non-insulating material (P-type body tie region BT in fig. 5a). Additionally, Houston discloses (col. 9, lines 8-18) that it is beneficial to not tie a potential to the bodies of the transistor.

In re claims 11 and 13, Houston discloses (col. 9, lines 35-43) that the bodies are electrically coupled by a connection of non-insulating material (P-type semiconductor body tie region BT in fig. 5a).

In re claims 12 and 15, Houston discloses (col. 17, lines 20-37) that the invention is used in an analog circuit stage which comprises a current mirror. The stage is a matched pair of current-sourcing P-channel transistors since figure 5a shows that the

source/drain regions are n-type and the channel is p-type for both transistors T4 and T5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flaker et al. (US 6,133,608) as applied to claim 6 above, and further in view of Houston et al. (6,037,808).

In re claims 7, and 8, Flaker et al. shows all of the elements of the claims except the circuit stage being transistors in a current mirror. Flaker discloses that the invention having the body link is beneficial in differential amplifiers. Houston discloses (col. 17, lines 20-37) that a body tie is used in an analog circuit stage which comprises a differential amplifier having a current mirror. The stage is a matched pair of current-sourcing P-channel transistors since figure 5a shows that the source/drain regions are n-type and the channel is p-type for both transistors T4 and T5). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the matched transistor pair of Flaker by incorporating a current mirror because Houston teaches that current mirrors may also benefit from transistor matched pairs that use body ties.

Allowable Subject Matter

Claims 1-5 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not show an integrated circuit semiconductor-on-insulator structure comprising a pair of matched transistors in a circuit stage that requires matched behavior of said pair, and a physical connection of semiconductor material which provides thermal conduction between respective bodies of the pair of transistors, but does not carry current during normal operation. As stated in the applicant's arguments, the body link (32) shown in Flaker provides an electrically conductive bridge. Furthermore, the body link allows two transistors eliminate any threshold voltage mismatch (col. 3, lines 67 – col. 4, line 10).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed with respect to claims 1-5 have been fully considered and are persuasive. The rejection of claims 1-5 has been withdrawn.

Applicant's arguments filed with respect to claims 6-19 have been fully considered but they are not persuasive. The applicant primarily argues that Flaker and Houston do not teach a physical connection of semiconductor material which provides thermal conduction between respective bodies of a pair of transistors. The examiner believes that both references teach the claimed limitations.

In the re the arguments for claim 6 and 16, the examiner believes that Flaker teaches that a physical connection of metallic material provides thermal conduction between transistors. Although the applicant is correct in asserting that Flaker's metal link provides electrical conduction, the applicant is not correct in assuming that the metal link does not provide thermal conduction. Many material placed between two bodies will provide thermal conduction. If a material provides electrical conduction then it also provides thermal conduction. In fact, metals naturally have the properties of electrical conduction and thermal conduction. Because Flaker teaches the use of metal to provide an electrical link between transistors, then Flaker inherently teaches that link provides thermal conduction.

In re the arguments for claim 10, the examiner believes that Houston also teaches that the physical connection of non-insulating material provides thermal conduction between respective bodies. As stated before, many materials placed between two bodies will provide thermal conduction. Because Houston satisfies the requirements of the claims in that a non-insulating material is formed between the bodies, then the body tie of Houston is also inherently thermally conductive. Therefore, the cited references show all of the elements of the claims and this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
July 23, 2004

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800